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Three Dimensional Integrated Circuit (3d IC): An Overview

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Abstract:

A three-dimensional Integrated circuit (3d IC) is a chip in which two or more layers of dynamic electronic mechanics are coordinated both vertically and horizontally into a single circuit. The promising three-dimensional (3d) assimilation technology is one of the emerging solutions to conquer the boundaries in interconnect scaling, accordingly offering a chance to proceed with execution upgrades utilizing CMOS technology. As the manufacture of 3d incorporated circuits has gotten reasonable, creating CAD instruments and structural systems are basic for the fruitful selection of 3d Integration technology. In this article, we first give a short definition about 3d IC, and it's important. Then brief some advantages, dis-advantage, benefit and challenges of 3D IC. And lastly present the architecture and manufacturing technology performance of 3D IC Technology.

Key words: 3DIC concept, Importance, Benefit & Challenge, 3D IC architecture, performance of 3D IC

Introduction

The innovation of integrated circuit technology keeps on scaling to more modest peculiarity sizes, enhancing the execution of doors. However, in light of the fact that worldwide interconnects don't scale accordingly with innovations; they

have turned into a significant execution and power bottleneck. As the technology scales, results are required that can conquer the confinements of wiring necessities for present and future chip plans. A three-dimensional integrated circuit is a chip in which two or more layers of active electronic components are integrated both vertically and horizontally into a single circuit. It offers an alluring answer for conquering the hindrances to interconnect scaling, along with offering a chance to proceed with execution upgrades utilizing CMOS engineering, with a littler structure element, higher integration thickness, and the backing for the realization of mixed technology chips.

The vast development of Information & communication industry is relying upon VLSI circuits with expanding usefulness and execution at least cost and power dissemination and 2d Ics create different gate delays and interconnection delay. In order to minimize these delays and total power consumption these technologies have been introduced, at first Intel introduced 80 core chip in 2007 in which run the frequency of 1.4GHz.

Concept of 3 D IC

The large development of computer and information technology industry is completely relying on VLSI circuits with expanding functionality and execution at least cost and power dissipation and 2D ICs create different gate delays and interconnection delay. In order to reduce these delays and total power consumption, 3D IC technology is introduced. From the beginning Intel presented a 80core chip in 2007 which run at the recurrence of 1.4 Ghz.

As we attempt to expand the complexity of chip design expands and this needs more and more transistors. So the final size of the circuit and delays expands. The losses inverses with large interconnection owing to the capacitance and safety are produced in the middle of the clad and copper. 3D IC is a

concept that can fundamentally enhance interconnect performance, increase transistor packing density, reduce chip area and power dissipation. In 3D design structure the entire chip "Si" is divided by the number of layers of oxide and metal to form transistor.

Importance of 3D IC

It is important to clarify that multiple-die packages have been around for a number of years. What is meant by "3D IC." Technologies such as wire-bonded system -in package (SiP) and multi-chip module (MCM) have been used since the 1990s to refer to packages in which numerous die is mounted on a typical substrate. With packaging- package (PoP), one section may be mounted on an alternate part.

Wire holding limits Sip execution, acquire space, and consumes important power. A silicon interposer layer can give much better, and a lot of debt to die interconnection. A silicon interposer might incorporate TSVs to give associations between die on both sides, or between upper metal layers and extra backside metal layers. The utilization of a silicon interposer with side-by-side die is regularly alluded to as "2.5d" stacking.

Stacked die designs are as of now utilized for huge memories today. On the other hand, the true estimation of 3d Ics will be acknowledged when heterogeneous die is bundled together for instance logic plus memory, or analog/RF plus MEMS.

As we endeavor to assemble the multifaceted chip configuration grows and this obliges more transistors. So the last size of the circuit and deferrals increases. The failures inverses with expensive interconnection in light of the way that the capacitance and safety are made amidst the clad and copper. 3d IC is a concept that can combine upgrade interconnect execution, extend transistor pressing thickness, diminish chip range and force scattering. In 3d setup structure

the entire chip "Si" is divided by the amount of layers of oxide and metal to structure transistor.
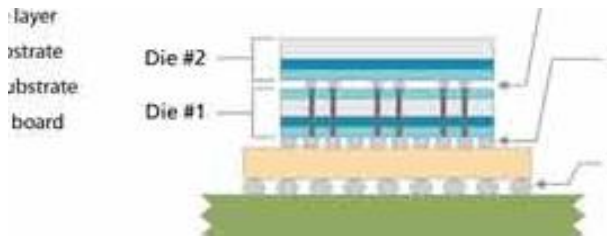

Figure 1 3D IC with two die

Advantage of 3D IC

3D IC is offering many potential advantages compared to traditional, 2d Socs. A portion of the key advantages as follows

> **Reduced mixed-signal challenges**
3D die stacks can leave analog and RF circuitry at a mature process node, such as 90nm or 130nm, where proven IP is available and manufacturing challenges are reduced.
Sensitive analog circuitry and noisy digital circuitry can now be kept separate.

> **Increased performance, lower power**
Shorter interconnect delays allow faster interconnect speeds and wider busses between logic and memory, helping meet bandwidth requirements.
Power and latency are reduced because big I/Os are no longer needed.
> Miniaturization, making 3D ICs appealing for compact mobile devices.
> Proven die-level IP can be used, taking the concept of "IP reuse" to an entirely new level.
> Digital and analog circuits can be formed with better noise performance
> It's more cost effective than 2D integration

> ➢ Expanded memory capacity
> ➢ Bus turn around time will reduce (Improved bus efficiency)
> ➢ Active termination power reduction ; Lower power consumption

Figure 2 shows a comparison of several different implementation choices, including 3D stacks with TSVs on the far right.
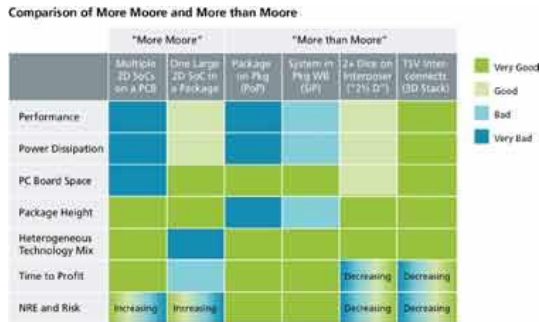

Figure 2: 3D ICs with TSVs offer the best performance, power, and density characteristics.

Disadvantage of 3D IC

The followings are some disadvantages as follows:

- Higher cost
- It drill holes/Fill plug by metal/Put bumps
- Thinning
- Handling/Align
- 2 types of die (Master and Slave)
-

Benefits and Challenges of 3D Integration

Staking ICs and densely interconnection them vertically carries a lot of benefits for the end product. However, the technology to take multiple planner die and perform the actual stacking and operational interconnection has not been completely ironed out yet. Moreover, a number of business challenges remain before

the supply chain for the production of 3D SICs is fixed. The next paragraphs outline these benefits and challenges and set the stage to understand why chip stacking is considered so important a step in integration as well as the remaining challenges that need to be addressed before this technology can become mainstream.

Benefits

Heterogeneous Integration

Typical consumer devices include a number of heterogeneous functionalities, like processing, sensing, memory, data transmission, which cannot be incorporated in a single die, because the underlying process technologies need to be optimized for the individual purposes. Chip stacking offers an alternative to board-level connectivity and system- in package solutions which suffer from reduced interconnection density between the functionalities and increased board footprint, hence cost. Does can be manufactured in different process technologies, even in different foundry lines or by completely different vendors and can be bonded at a later stage by a third party. This enables, for example, to stack DRAM memory on logic processing or analog and RF functionalities with baseband processing on a single chip. The increased interconnection density opens up new opportunities for efficient system integration.

High Degree of Integration in a small form factor

A Strong trend to miniaturize consumer electronic product is evident now a days, thickness of the devices has even become a selling proposition for a new generation of smart-phones and tablets. This trend puts significant pressure on chip providers to add the chip form factor as another design optimization criterion. In order to make devices ever thinner, with the screen, and the printed circuit board taking up a significant

amount of z-axis real estate, the chips need to be less than a couple of millimeters thick. Moreover, consumer electronics manufacturers are pushing chip vendors to increase the functionality per chip in order to reduce the component count on the printed circuit board and cost as a result. Stacking of thinned chip is the only technology available currently that can densely pack more functionality than ever before into a very thin package. This may be the key to enable the next wave of consumer electronics miniaturization.

Improved Power Consumption

Power consumption is the second most important design optimization criterion after cost nowadays. Chips that are embedded in portable devices need to consume power in a very frugal manner in order to maximize battery lifetime between recharges. Power consumption is becoming ever more important for other application as well. computer farms and personal computers need to regulate their power consumption to control temperature and avoid catastrophic side-effects to the chips consumption to control temperature and avoid catastrophic side-effects to the chips themselves. Manufacturers of set top boxes and other similar devices need components that are power efficient to avoid installing cooling equipment which increases cost. One of the main sources of power dissipation on chips is the wires interconnecting the various functional blocks of the chip. As more and more functionality is integrated on a chip and physical dimensions increase, these wires tend to get longer and more power hungry as a result, since they need to transmit more information, faster, over larger distances. Continuing this trend using conventional planar chip leads to bottleneck. Chip stacking offer an alternative solution. Partitioning the functionality of the chip in multiple die and vertically stacking them increases the locality between the different functional blocks. Blocks that previously were on opposite sides of a planar die can now be placed on top of each

other. This enables a severe of a planar die can now be placed on top of each other. This enables a severe reduction of interconnect lengths which directly translates to reduced power consumption or even faster data transmission if necessary.

Cost Benefits

Cost is the single most important driver and optimization target in the design of integrated circuits for the most applications. Traditional semiconductor scaling techniques that have enabled the increased system integration up to now are becoming more difficult and more expensive with each new technology node. The cost of developing the process technology and building a foundry for the next node is becoming so expensive that only very few companies can afford it world wide. Apart from sheer capital expenditure, yield is also becoming a bottleneck for chip production,. Defects that reduce yield in the production process are not scaled in size together with the feature dimensions of chips and clean rooms cannot become any cleaner, the defect density has saturated. Dies become bigger to accommodate more functionality and as a consequence yield is dropping. This further increases the cost of producing chips in each next technology node, since fewer of them will be functional. Chip stacking offers an alternative route to integration, which may prove to be more cost-efficient First, it enables the stacking of multiple dies, which means that large, low-yielding die can be split into smaller ones which will then be bonded together. Second, If some part of the system has more relaxed requirements than the critical one, it can be manufactured in an older, cheaper technology node to further reduce the overall cost. Hence there is great potential for cost optimization as long as additional process steps added in the process for bonding the multiple die together are cheap enough! This is one of the major challenges that must overcome in order for chip stacking to become a mainstream technology, which

will complement traditional CMOS to enable the next stores of
scaling for the semiconductor industry.

Technical Challenges

The potential benefits of chip stacking are too lucrative to
ignore, Semiconductor companies, research centers and
universities are spending significant time in an effort to
address the following reaming technical challenges and make
chip stacking a reality.

Process Steps

Stacking multiple chips, obviously require additional process
steps. These steps can be clustered into three main functions,
namely through silicon via (TSV) etching and filling, thinning
and bonding. TSVs are the vertical interconnections between
the different die, they connect an interconnect of the die where
they are created to an interconnect on the die just below in
order to establish an electrical connection. Creating them
requires to etch holes through the silicon substrate in the
appropriate die during its manufacturing and to later fill these
holes up with conductive material. Thinning refers to a process
step that thins the wafer with the TVSs to a thickness ranging
from few tens of micrometers to a few hundred micrometers.
This is an essential step in order to create a 3D SIC with a
small thickness. The third important step is bonding were die
are bonded together in pairs. This requires the careful
alignment of the two die and their bonding such that the TSVs
will land at the correct places to establish electrical connections
with the lower die.

Operating Temperature

The operating temperature of chips is mainly determined by
three factors, the ambient temperature, the density of their
power consumption, and how they can transfer heat out of the
package. Power consumption creates heat and if it cannot be

dissipated fast enough the temperature of the die increases, leading to problems such as increased leakage currents in the transistors and reliability degradation. Stacking of multiple die affects the power consumption density and the capability of the chips to dissipate heat. The power density increases because multiple die are thinned and bonded together in a small volume. The capability to dissipate this heat depends on the materials used in the chips and the package. In a stacked IC, the heat has to be potentially dissipated through another die. The difference in heat conductivity needs to be understood and evaluated. The fact that the die in the stack is thinned before bonding adds another level of complication; thicker die can spread heat much better than thin ones along their horizontal plane. One school of thought believes that this increase in power density can lead to a temperature increase in the overall die stack. Another school believes that even in conventional planar chips the temperature problems are encountered in small hotspots; hence, the problem is essentially similar. It is clear that some research is needed to compare the heat dissipation capabilities of conventional vs stacked integrated circuits in the context of their packages and to assess the impact of how and where heat is generated on the operating temperature of the die.

Mechanical Stability

Three-dimensional chip stacks will comprise a number of die of different sizes, thinned to a few tens of micrometers, made of different materials stacked and bonded on top of each other so as to retain electrical connections. This system presents a nightmare in terms of mechanical stability when temperature changes. Different materials, and as a result different die, have thermal expansion coefficients and are affected in a different manner by temperature gradients. This creates a potential threat that the stack might partially de-bonded if temperature changes fast, which might be a catastrophic failure electrical

connection may be jeopardized. Mechanical stress that builds up this source can have subtler effects as well. Stress engineering has been widely used in deep sub-micron technology nodes to improve the electrical properties of transistors. Mechanical stress due to thermal expansion can interfere with the stress carefully engineered in the transistor channel to destroy the on-currents of transistors. Another major source of problems is the handling of the thinned wafers. After thinning, wafers are so thin that they actually become flexible. Extreme care needs to be taken to make sure they are transferred from on a process step to the other without damaging them. The current solution for handling such wafers is to attach them to supporting carrier wafers, but even the operations of bonding and de-bonding them to and from the carrier wafers may create mechanical issues.

Testing

Testing is very important, though often underestimated; step in the chip manufacturing process. Any manufacturing plat wants to ship only operational products; hence, testing is critical. Testing the functionality and performance specifications of a 3D chip stack is similar to testing a conventional chip. Chip stacking however, offers opportunities to test the individual die before they are bonded together. In order to avoid bonding functional with nonfunctional die together, which leads to wasting functional die, each die should be tested separately. This adds another level of complication to the testing process. Moreover, testing individual thinned die is a tricky process as their mechanical probing is an extremely difficult process. Research is needed to establish a proper testing protocol for chip stacks and a way to test the individual die before bonding to increase yield and minimize cost. Design for testability is another area of testing that may be affected by three – dimensional integration. It comprises techniques to embed testing functionality, scan-chains for instance, in the chip so as

to efficiently test it. Partitioning the system functionality in multiple separate die can increase the complexity of such techniques, this impact needs to be better understood.

Bonding Strategies

Three ways exist to perform the bonding that creates chip stacks: wafer to wafer, die to wafer, and die to die, Each of these alternatives has clear advantages and disadvantages. Wafer to wafer bonding is the fastest, since multiple stacks are created at once, but the different die in the stack have to exactly the same shape of size. Die to wafer bonding is an intermediate solution where one wafer has been diced and individual die is bonded on the second wafer. This makes alignment more difficult, but it enables stacking of die with different physical dimensions and allows to pretest the die and to create stacks of functional die. Die to die bonding offers the most freedom to the foundry to mix and match operating die to create chip stacks. It is the least preferred approach, however, since it increases production time and cost significantly. Depending on the type of product any of the aforementioned approaches may be useful. Even wafer to wafer bonding which may result

Architecture for 3D IC

3-D ICs have recently attracted great interest from researchers and IC designers. Studies demonstrate a potential performance improvement of up to 65% by transferring a placement from 2-D to 3-D and eliminating long interconnects. Furthermore, the multiple device layer structure of 3-D ICs provides a platform to integrate different components, such as digital ICs, analog ICs, memory, RF modules, and different technologies such as SOI, SiGe HBTs, GaAs, etc., into one single circuit stack. Thus, it is a more flexible vehicle for system-on-chip (SoC) and system-in-package (SiP) designs compared to planar 2-D IC technologies.

Although 3-D integration shows promise, significant challenges associated with the efficient circuit design and operation have hampered its adoption and further development. The most important issue in 3-D IC is heat dissipation. The thermal problem has already had an impact on the reliability and performance of high-performance 2-D ICs. The problem is aggravated in 3-D ICs, principally for two reasons: the devices are more packed, which results in higher power density; and the insulating dielectric layers between the device layers have much lower thermal conductivities than silicon. Furthermore, the third dimension brings both flexibility and difficulties to physical design algorithms. The existing 2-D metrics cannot be simply extended to generate similar metrics for 3-D designs. Take wavelength as an example: a bounding-cube" might not have enough accuracy for wirelength estimation because of the existence of huge obstacles in z-direction. Also, a 3-D IC physical design problem is usually of higher complexity, with a much enlarged solution space due to the multiple device layer structure. Efficient 3-D physical design tools, including 3-D floorplanning, placement and routing tools, that are specifically designed to take the thermal problem into consideration, are essential to 3-D IC circuit design.

The following figure shows the 3-D physical design tool package that we are working on. Among the three major modules, we have completed the initial version of the floorplanning and routing tools and are working on the placement tool. Our group has also developed MEVA-3D, an automated physical design and architecture performance estimation flow for 3D architectural evaluation, which includes 3D floorplanning, routing, interconnect pipelining and automated thermal via insertion, and associated die size, performance, and thermal modeling capabilities.
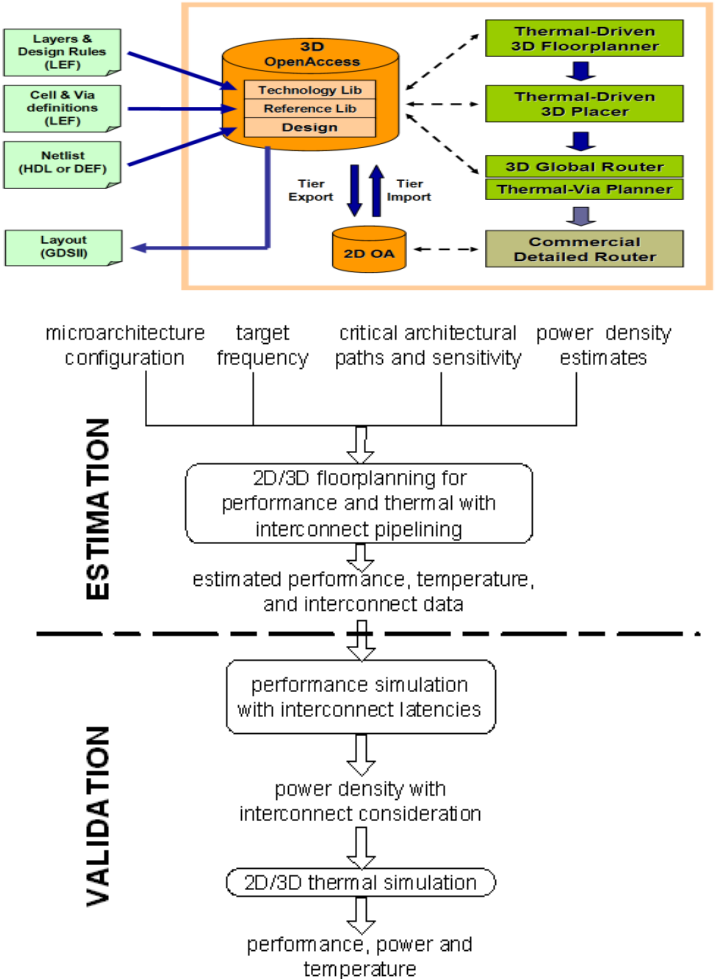
Figure-3 Architecture of 3D IC Design

We are also exploring novel 3D architectures. We have proposed the accelerator-over-processor computing platform as shown below. The accelerators in this architecture are designed for a specific domain. They can be shared among applications in the domain. It provides an easy way to extend a general-purpose processor to a domain-specific professor with significant performance improvement and energy savings. We also developed optimization methodologies to maximize the gain under any given area/bandwidth constraints.
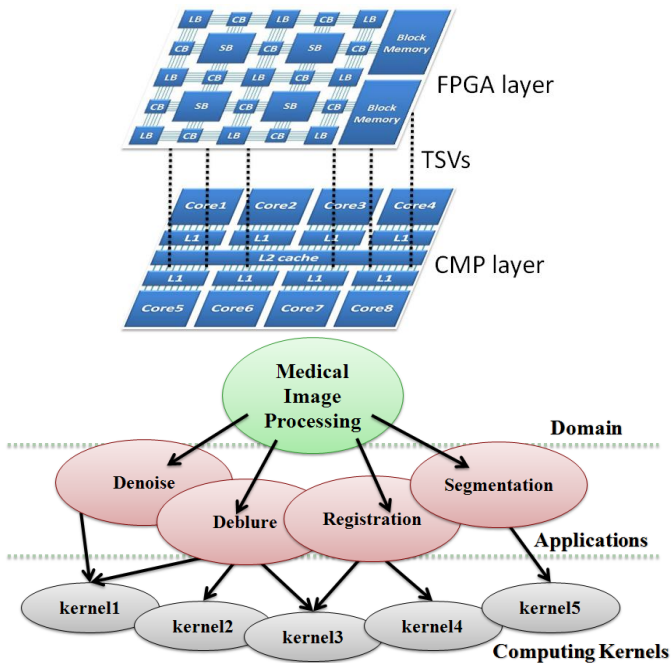
Figure-4 Manufacturing technology for 3D IC

For Building 3D IC, there are 4 ways as follows:

Monolithic

In monolithic, electronic segments and their associations (wiring) are implicit layers on a solitary semiconductor wafer, which is then diced into 3D ICs. There is a substrate, henceforth no requirement for adjusting, thinning, bolding, or through-silicon vias. A current defeated the methodology temperature restriction by partitioning the transistor manufacture to two stages. A high temperature stage, which is carried out before layer transfer follow the take after by a layer exchange use particle cut, known as layer transfer that has been the prevailing system to create SOI wafers for as far back as two decades. Various thin (10s–100s nanometer scale) layers of virtually defect free Silicon might be made by using low temperature (<400c) bond and divide strategies, and set on top

of dynamic transistor circuitry. Follow by finishing the transistors utilizing etch and deposition forms. This monolithic 3d-IC innovation has been examined at Stanford University under a DARPA-sponsored grant
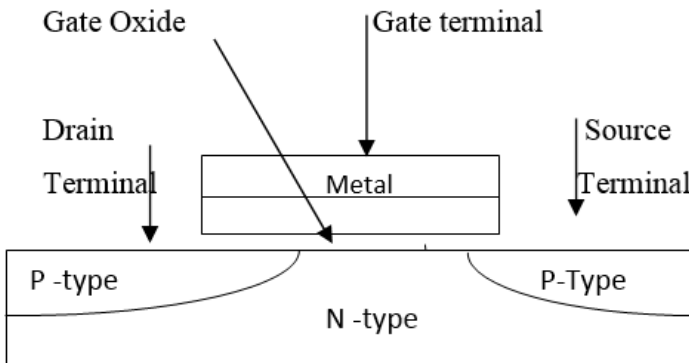

Figure-5 Monolithic

Wafer-on-Wafer

In this method the components of electronic are based on two or more semiconductor wafers, which are then adjusted, reinforced, and diced into 3d ICs. Each wafer might be thinned before or after bonding. Vertical associations are either incorporated with the wafers before bonding or else made in the stack after bonding. These "through-silicon vias" (Tsvs) pass through the silicon substrate(s) between dynamic layers and/or between a dynamic layer and an outer bond pad. Wafer-on-wafer bonding can reduce yields, since if any 1 of N chips in a 3d IC are blemished, the whole 3d IC will be imperfect. Also, the wafers must be the same size, yet numerous exotic materials (e.g. III-Vs) are made on much littler wafers than CMOS logic or DRAM (commonly 300 mm), complicating heterogeneous integration.

Die-on-Wafer

In this method, electronic segments are based on two semiconductor wafers. One wafer is diced; the singulated s dice

are adjusted and fortified onto die sites of the second wafer. As in the wafer-on-wafer system, thinning and TSV creation is performed either before or after bonding. Extra dice may be added to the stacks before dicing.
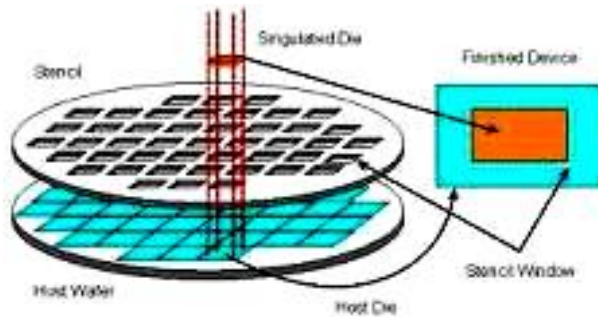

Figure-6 Die on Wafer

Die-on-Die

In this method, electronic parts are based on different dice, which are then adjusted and bonded. Thinning and TSV creation may be carried out before or after bonding. One advantage of die on die is that every segment die could be tried in the first place, so that one bad die does not destroy a whole stack. Moreover, each one die in the 3d IC might be binned beforehand, so they could be blended and matched to upgrade power consumption and performance (e.g. Matching various dice from the low power methodology corner for a mobile application).

Performance of 3D IC

3D technology enables the memory arrays to be placed above or under logic circuitry, resulting in an increased bandwidth and thus a significant performance gain in communication between memory and microprocessor. In particular, as the amount of on-chip memory increases (i.e., the majority of the chip will soon be occupied by memory), the latency of the path of logic to memory becomes a limiting factor in the logic-memory system. The ability to stack logic and memory has been demonstrated.

In addition, one can determine maximum system performance as a function of the number of device layers. Maximum performance depends on power dissipation constraints. In the presence of power constraints, there are global technology scaling optima that yield maximum computation (for example, if devices are scaled too far, leakage consumes too much of the power). Simple models of device and system dependencies have been developed, and optimizations have been performed. These layering models ignore the impact of blockage due to signals passing through a device layer. As depicted in Figure 3 the results show significant potential advantage for 3D integration, with performance, increasing roughly as the square root of the number of circuit layers that are stacked. For these data points, device characteristics (i.e Vdd,VT,tox, gate length, mean FET width, wire half-pitch, and repeater spacing) have all been optimized for maximum performance where performance is calculated as Performance ¼ total number of logic switching events per second in a processor core.

Conclusion

3D ICs is the first of a new generation of thick, expensive chips having less delay and interconnection losses that will replace the conventional storage and recording media. It has emerged as a key empowering technology to expand the scaling trajectory anticipated by Moore's law. However, their prosperity and commercial feasibility will depend to a significant extent on their production yields and the corresponding test solutions for ensuring them, which, at of right now, are left normally unexplored in the research community. In this article, we have presented few benefit, challenges, advantage and disadvantages of 3D ICs. Further, it is narrated in the architecture of 3D IC, Manufacturing technology and performance of 3D ICs. This

technology can be widely adopted and become a market success. It is a relief to interconnect driven IC design.

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